DATA SHEET

MAX708R/S/T

3 V microprocessor supervisor circuit with power fail comparator and manual reset

Product data
Supersedes data of 2003 Aug 08

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Philips
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3 V microprocessor supervisor circuit with power fail comparator and manual reset

MAX708R/S/T

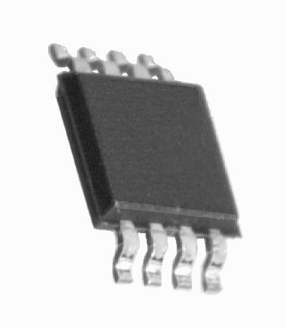
DESCRIPTION

The MAX708R/S/T are microprocessor supervisory circuits used to monitor +3 V power supply levels in +3 V to +5 V microprocessor and other logic systems. The R, S, T suffixes have reset thresholds of 2.63 V, 2.93 V and 3.08 V, respectively. They reduce the number of circuit components, and improve reliability and accuracy compared to using separate ICs or discrete components.

The MAX708R/S/T features make the MAX708R/S/T ideal for use in portable, battery operated equipment. The low supply current, typically 50 μA, minimizes battery load. Both $\overline{\text{RESET}}$ and RESET are active during power-up, power-down and brownout conditions An active-LOW manual reset input is also available.

A 1.25 V threshold detector provides power-fail warning. This independent comparator can be used to monitor a second voltage supply and provide an early warning to the microprocessor that voltage is falling. This allows for an orderly shutdown, transmitting an alert to an operator, or activation of an alternate power source before the device asserts the reset signals.

The device is available in the 8-pin SO package (SOP005).



FEATURES

- RESET and $\overline{\text{RESET}}$ signals
- Independent comparator with 1.25 V threshold for power failure or low battery warning
- Manual reset input
- 50 μA quiescent current
- Reset thresholds of 2.63, 2.93, and 3.08 V
- Guaranteed RESET assertion to V_{CC} = 1 V

APPLICATIONS

- Battery powered devices
- Critical microprocessor monitoring
- Controllers
- Portable instruments

SIMPLIFIED SYSTEM DIAGRAM

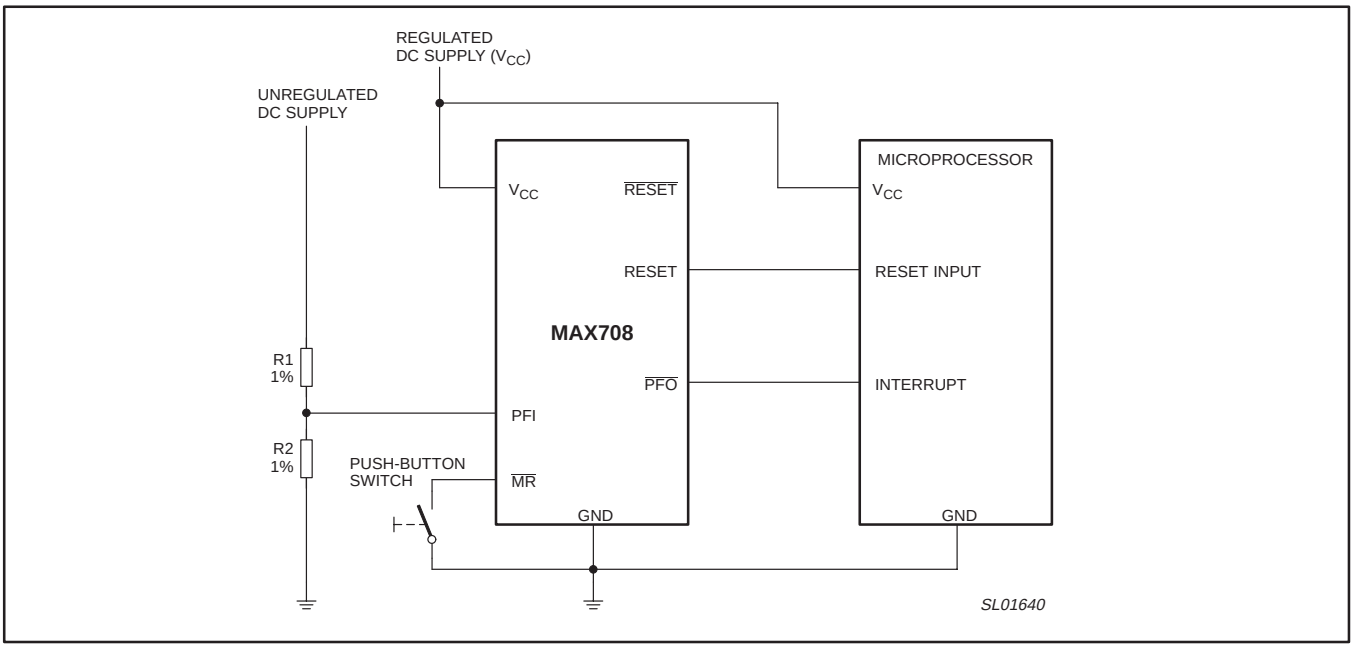


Figure 1. Simplified system diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE
	NAME	DESCRIPTION	VERSION	
MAX708**x**D	SO8	plastic small outline package; 8 leads (see dimensional drawing)	SOP005	–45 °C to +85 °C

NOTE:
The device has 3 voltage output options, indicated by the **'x'** on the 'Type number'.

Part number	Threshold Voltage (Typical)
MAX708RD	2.63 V
MAX708SD	2.93 V
MAX708TD	3.08 V

Marking code

Each device is marked with a four letter code. The first three letters designate the product. The fourth, represented by an 'x', designates the date tracking code.

Part	Marking
MAX708RD	ANEx
MAX708SD	ANDx
MAX708TD	ANCx

PIN CONFIGURATION

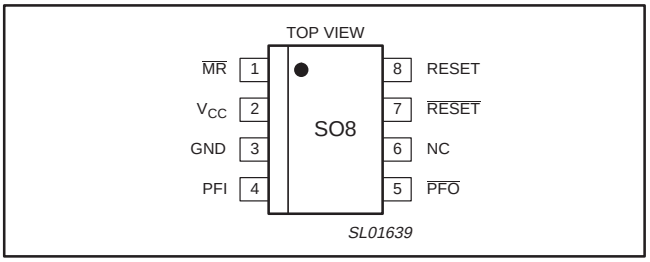


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	$\overline{MR}$	Manual reset input (Active-LOW). Triggers a reset pulse when pulled below 0.6 V. Connect to V_{CC} or leave floating if not used.
2	V_{CC}	Supply voltage input.
3	GND	Ground.
4	PFI	Power fail comparator input. When PFI is less than 1.25 V, $\overline{PFO}$ goes LOW, otherwise $\overline{PFO}$ remains HIGH. Connect to ground if not used.
5	$\overline{PFO}$	Power fail comparator output (Active-LOW). When voltage at PFI is less than 1.25 V, $\overline{PFO}$ goes LOW and sinks current. Do not connect if not used.
6	NC	No connection.
7	$\overline{RESET}$	Active-LOW reset output. $\overline{RESET}$ is LOW if V_{CC} is below the threshold voltage or if $\overline{MR}$ is held LOW. $\overline{RESET}$ is maintained for 200 ms after the reset conditions are terminated.
8	RESET	Active-HIGH reset output. RESET is HIGH if V_{CC} is below the threshold voltage or if $\overline{MR}$ is held LOW. RESET is maintained for 200 ms after the reset conditions are terminated.

MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage		–0.3	6.0	V
V_n	Other input pin voltage	Note 1	–0.3	V_{CC} + 0.3	V
	Input current at V_{CC} or GND		–	20	mA
	Output current, all outputs		–	20	mA
	Rate of rise at V_{CC}		–	100	V/µs
T_{amb}	Ambient temperature		–40	+85	°C
T_{stg}	Storage temperature		–65	+160	°C
P	Power dissipation, SO8 package	T_{amb} = 70 °C; Note 2	–	470	mW

NOTES:
1. Input voltage limits on PFI and $\overline{MR}$ can be exceeded provided the input current is less than 10 mA.
2. Derate the dissipation 5.88 mW/°C above 70 °C.

ELECTRICAL CHARACTERISTICS

T_{amb} = –40 °C to +85 °C; V_{CC} = ($V_{RST(max)}$ + 0.7 V) to 5.5 V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{CC}	Operating voltage range			1.2	–	5.5	V
I_{SUP}	Supply current	V_{CC} < 3.6 V		–	50	300	µA
		V_{CC} < 5.5 V		–	65	500	µA
V_{RST}	Reset threshold (Note 1)	MAX708R		2.55	2.63	2.70	V
		MAX708S		2.85	2.93	3.00	V
		MAX708T		3.00	3.08	3.15	V
	Reset threshold hysteresis			–	20	–	mV
t_{RST}	Reset delay time (Note 1)	MAX708R; V_{CC} = 3.0 V		140	200	280	ms
		MAX708S, MAX708T; V_{CC} = 3.3 V		140	200	280	ms
		MAX708R, MAX708S, MAX708T; V_{CC} = 5.0 V		–	200	–	ms
V_{OH}	HIGH-level output voltage	$\overline{RESET}$	$V_{RST(max)} < V_{CC} < 3.6V$; I_{SOURCE} = 500 µA	$V_{CC} \times 0.8$	–	–	V
			4.5 V < V_{CC} < 5.5 V; I_{SOURCE} = 800 µA	V_{CC} – 1.5	–	–	V
		RESET	$V_{RST(max)} < V_{CC} < 3.6V$; I_{SOURCE} = 500 µA	$V_{CC} \times 0.8$	–	–	V
			4.5 V < V_{CC} < 5.5 V; I_{SOURCE} = 800 µA	V_{CC} – 1.5	–	–	V
		$\overline{PFO}$	$V_{RST(max)} < V_{CC} < 3.6V$; I_{SOURCE} = 500 µA	$V_{CC} \times 0.8$	–	–	V
			4.5 V < V_{CC} < 5.5 V; I_{SOURCE} = 800 µA	V_{CC} – 1.5	–	–	V
V_{OL}	LOW-level output voltage	$\overline{RESET}$	$V_{RST(max)} < V_{CC} < 3.6$ V; I_{SINK} = 1.2 mA	–	–	0.3	V
			4.5 V < V_{CC} < 5.5 V; I_{SINK} = 3.2 mA	–	–	0.4	V
			V_{CC} = 1.2 V; I_{SINK} = 100 µA	–	–	0.3	V
		RESET	$V_{RST(max)} < V_{CC} < 3.6$ V; I_{SINK} = 500 µA	–	–	0.3	V
			4.5 V < V_{CC} < 5.5 V; I_{SINK} = 1.2 mA	–	–	0.4	V
		$\overline{PFO}$	$V_{RST(max)} < V_{CC} < 3.6$ V; I_{SINK} = 1.2 mA	–	–	0.3	V
			4.5 V < V_{CC} < 5.5 V; I_{SINK} = 3.2 mA	–	–	0.4	V
	$\overline{MR}$ pull-up current	$V_{RST(max)} < V_{CC} < 3.6$ V; $\overline{MR}$ = 0 V		25	70	250	µA
		4.5 V < V_{CC} < 5.5 V; $\overline{MR}$ = 0 V		100	250	600	µA
t_{MR}	$\overline{MR}$ pulse width	$V_{RST(max)} < V_{CC} < 3.6$ V		500	–	–	ns
		4.5 V < V_{CC} < 5.5 V		150	–	–	ns
V_{IL}	$\overline{MR}$ LOW-level input threshold	$V_{RST(max)} < V_{CC} < 3.6$ V		–	–	0.6	V
		4.5 V < V_{CC} < 5.5 V		–	–	0.8	V
V_{IH}	$\overline{MR}$ HIGH-level input threshold	$V_{RST(max)} < V_{CC} < 3.6$ V		$V_{CC} \times 0.7$	–	–	V
		4.5 V < V_{CC} < 5.5 V		2.0	–	–	V
t_{MD}	MR to reset out delay (Note 1)	$V_{RST(max)} < V_{CC} < 3.6$ V		–	–	750	ns
		4.5 V < V_{CC} < 5.5 V		–	–	250	ns
	PFI input threshold	PFI falling; MAX708R: V_{CC} = 3.0 V; MAX708S/T: V_{CC} = 3.3 V		1.2	1.25	1.3	V
	PFI input current			–25	0.01	+25	nA

NOTE:
1. Applies to RESET and $\overline{RESET}$.

TIMING DIAGRAM

On power-up, when V_{CC} reaches 1 V, $\overline{RESET}$ is guaranteed to be a logic LOW and RESET is guaranteed to be a logic HIGH.

Event A: V_{CC} rises to the reset threshold voltage, V_{RST}. At this time, the internal reset delay timer is initiated. $\overline{RESET}$ and RESET will remain asserted for the reset delay time, t_{RST} of typically 200 ms after the supply voltage rises above the reset threshold, V_{RST}.

Event B: At this time, the resets are released. $\overline{RESET}$ goes HIGH; while RESET goes LOW. The reset delay time helps to ensure valid reset signals despite erratic changes in supply voltage.

Events C–E: At Event C, under brown-out conditions, V_{CC} falls below the reset threshold minus the hysteresis voltage (typically 20 mV), and the reset signal is asserted. As power recovers and V_{CC} rises above the reset threshold (Event D), it once again initiates the reset delay time. At Event E, V_{CC} falls below the reset threshold before the reset delay time has elapsed and reset remains asserted.

Event F: The V_{CC} rises above the reset threshold again and remains above the reset threshold for typically 200 ms. At G, the reset is once again released.

Event H: The $\overline{MR}$ is externally pulled LOW for longer than 150 ns (minimum $\overline{MR}$ pulse width, t_{MR} for V_{CC} = +5 V).

Event I: The manual reset is asserted within 250 ns (maximum $\overline{MR}$ to reset out delay time, t_{MD} for V_{CC} = +5V).

Event J: the $\overline{MR}$ pin returns HIGH. At this point, reset delay timer is initiated and in typically 200 ms, (at Event K), the reset condition is released.

Event L: On power-down, when V_{CC} falls below V_{RST} – 20 mV, $\overline{RESET}$ and RESET are guaranteed to be asserted until V_{CC} falls below 1 V.

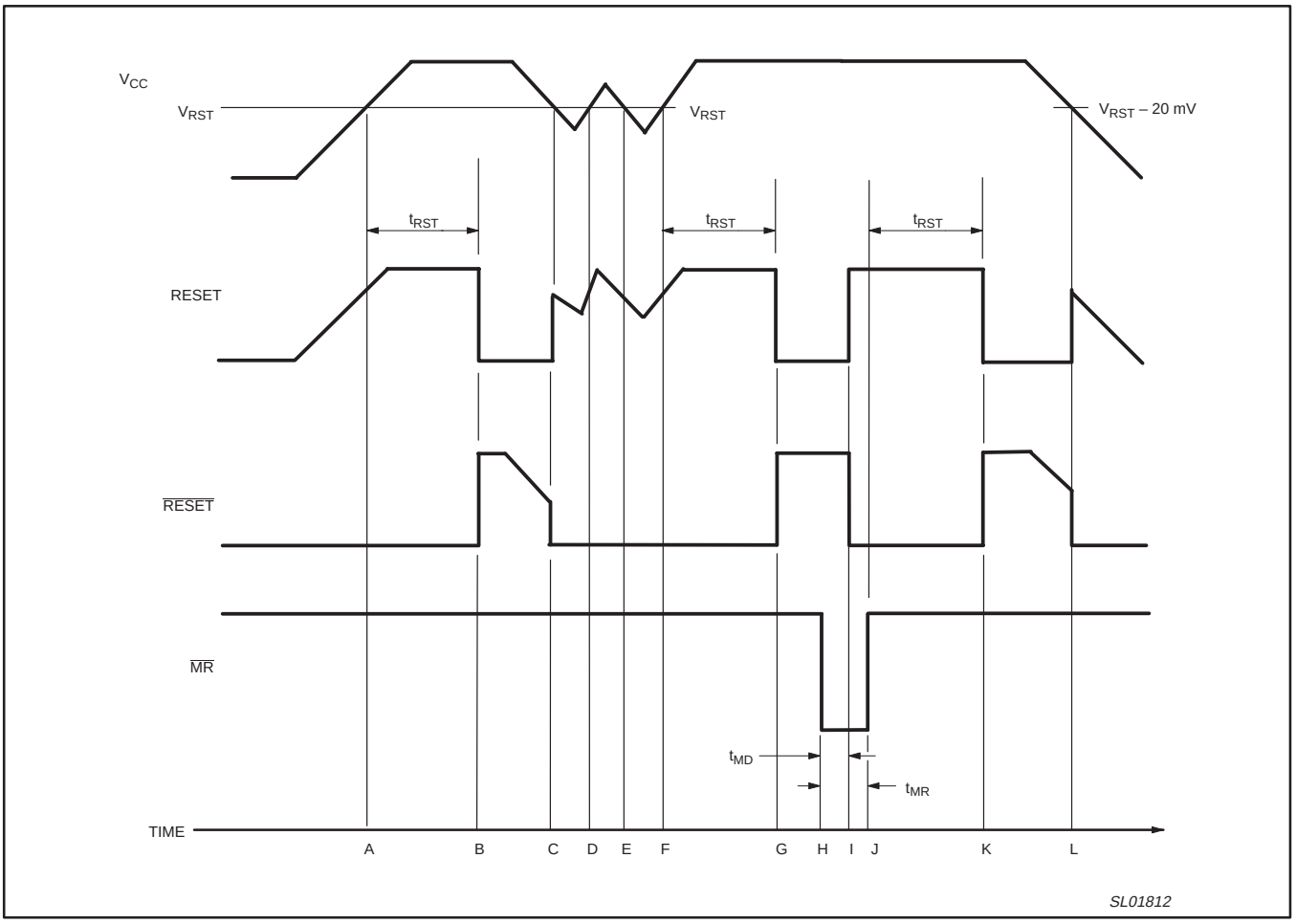


Figure 3. Timing diagram.

TECHNICAL DISCUSSION

General discussion

The MAX708R/S/T microprocessor supervisor circuits are comprised of both $\overline{\text{RESET}}$ and RESET outputs, a $\overline{\text{MR}}$ manual reset input, and a comparator which may be used for power-failure detection (see Figure 4).

The reset threshold voltages are guaranteed within ±3% of the nominal reset threshold. The MAX708R/S/T are designed to monitor +3 V to +3.3 V power supplies in +3 V to +5 V microprocessor and other logic systems. With a threshold voltage range between 5% to 10% of the nominal supply voltage, the MAX708R/S/T will assert an output within predictable range of power supply voltage.

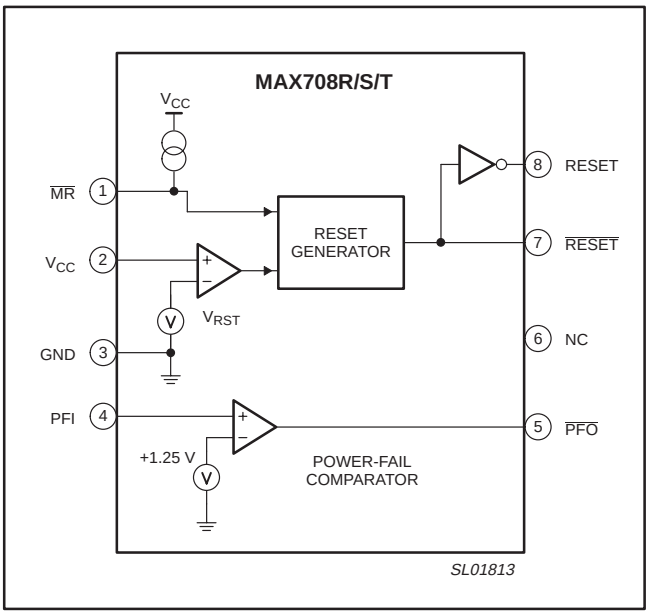


Figure 4. MAX708R/S/T internal block diagram.

$\overline{\text{RESET}}$ and RESET outputs

The MAX708R/S/T $\overline{\text{RESET}}$ and RESET outputs are push-pull outputs and do not require an external pull-up resistor. The $\overline{\text{RESET}}$ output is active-LOW logic, while the RESET output is active-HIGH logic.

Manual Reset

The manual reset input, $\overline{\text{MR}}$ is active-LOW logic. It allows the $\overline{\text{RESET}}$ and RESET to be asserted by a pushbutton switch. A mechanical pushbutton switch is effectively debounced by the 140 ms minimum reset time delay. $\overline{\text{MR}}$ may be driven from an external logic circuit because it is TTL/CMOS compatible. The minimum $\overline{\text{MR}}$ input pulse is 500 ns for V_{CC} = +3 V and 150 ns for V_{CC} = +5 V. If manual reset will not be used, leave the pin left floating or tie it to V_{CC}.

Power-fail comparator

The power-fail comparator has many useful purposes, such as monitoring upstream or secondary power supplies. The Power-Fail Output ($\overline{\text{PFO}}$) and the non-inverting Power-Fail Input (PFI) are pinned out. The inverting input of the power-fail comparator is internally connected to a 1.25 V reference. The comparator has 10 mV of hysteresis which prevents repeated triggering of the output ($\overline{\text{PFO}}$).

APPLICATION INFORMATION

Operating with a +3 V or +5 V supply

When powered from either +3.0 V or +5.0 V, the MAX708R/S/T provides voltage monitoring at the reset threshold. The MAX708R/S/T are ideal for portable applications that are powered from a +3 V battery or an AC-DC wall adapter that generates +5 V.

Power-fail comparator

An early warning power-fail circuit uses the power-fail input to monitor the upstream, unregulated DC supply that powers the +3 V/+3.3 V regulator powering the MAX708R/S/T.

Figure 1, “Simplified system diagram”, shows the resistor divider network that is connected to PFI. The network resistors R1 and R2 are chosen so that the voltage at PFI will fall below 1.25 V before the regulator voltage drops out. The PFO signal may be used to interrupt the microprocessor so it can perform an orderly shutdown.

Any unregulated or regulated supply can be monitored by adjusting the resistive divider for the desired power supply trip voltage. Table 1 shows examples for nominal trip voltages of 3.7 V and 10.9 V. The desired trip voltage, V_T is calculated by the following equation:

$$V_T = 1.25\ V\left[\frac{(R1 + R2)}{R2}\right]$$

Table 1. Power-fail detection circuit of 3.7 V and 10.9 V

	R1 1%	R2 1%	V_T
5 V unregulated power supply	1 MΩ	510 kΩ	3.7 V
12 V unregulated power supply	1 MΩ	130 kΩ	10.9 V

Adding hysteresis to the power-fail comparator

Hysteresis adds noise margin to the power-fail comparator and prevents repeated triggering of PFO when V_{IN} is varying around the comparator trip point. In Figure 5, “Adding hysteresis to the power-fail comparator”, R1 and R2 are the divider resistors that set the desired trip point. R3 is added from the comparator input to the output to increase hysteresis; it is typically an order of magnitude greater than R1 and R2. The current through R1 and R2 should be at least 1 mA to ensure that the 25 nA max PFI input current does significantly shift the trip point. Capacitor C1 provides noise rejection.

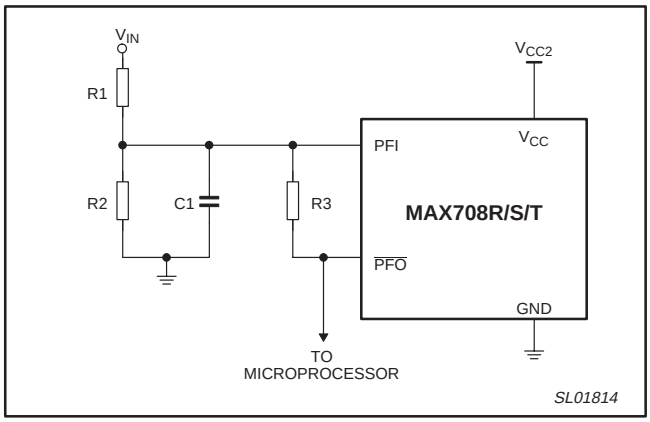
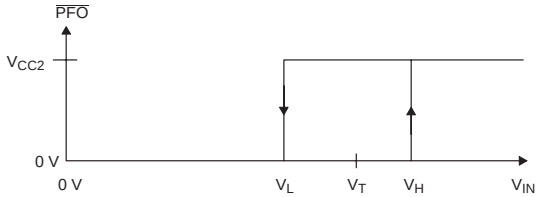


Figure 5. Adding hysteresis to the power-fail comparator.



$$V_T = 1.25\ V\left[\frac{(R1 + R2)}{R2}\right]$$

The hysteresis of V_H and V_L voltages are calculated by:

$$V_H = 1.25\ V\left\{1 + \left[\frac{(R3 + R2)}{(R2 \times R3)}\right] R1\right\}$$

$$V_L = 1.25\ V + R1\left\{\left(\frac{1.25}{R2}\right) + \left(\frac{(1.25 - V_{CC})}{R3}\right)\right\}$$

Thus,

$$V_{HYS} = V_H - V_L = \frac{(R1 \times V_{CC2})}{R3}$$

Monitoring a negative voltage

The power-fail comparator can be used to monitor a negative voltage using the circuit shown in Figure 6.

When the negative supply is operating in tolerance, $\overline{PFO}$ is LOW. However, when the negative supply drops (goes positive) $\overline{PFO}$ goes HIGH.

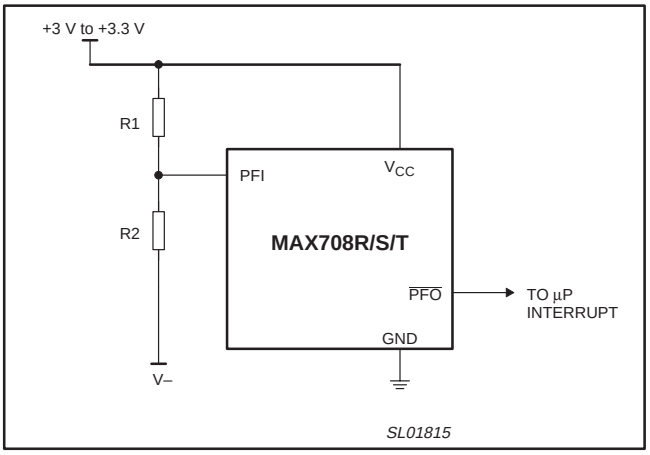


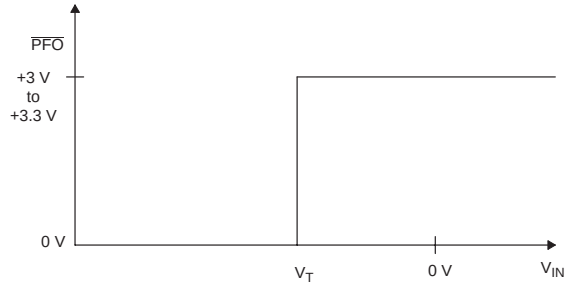
Figure 6. Circuit for monitoring a negative voltage.

When monitoring a negative supply, the trip voltage, V_T is a negative voltage. Use the following ratio to determine the divider resistors:

$$\frac{(V_{CC} - 1.25)}{R1} = \frac{(1.25 - V_T)}{R2}$$

Solving for V_T:

$$V_T = 1.25 - \left(\frac{R2}{R1}\right)(V_{CC} - 1.25)$$



Ensuring a valid reset down to V_{CC} = 0 V

When V_{CC} falls below 1 V, the MAX708R/S/T $\overline{RESET}$ no longer sinks current (i.e., it becomes open circuit). A high impedance CMOS logic input connected to $\overline{RESET}$ can drift to undetermined voltages. In most applications in which the microprocessor circuitry is inoperative below 1 V this will not present a problem. However, in applications in which $\overline{RESET}$ must be valid down to 0 V, use a relatively large pull-down resistor from $\overline{RESET}$ to ground (Figure 7). 100 kΩ is small enough to provide a path for any stray leakage currents to flow to ground (holding $\overline{RESET}$ LOW), while it is large enough not to load RESET.

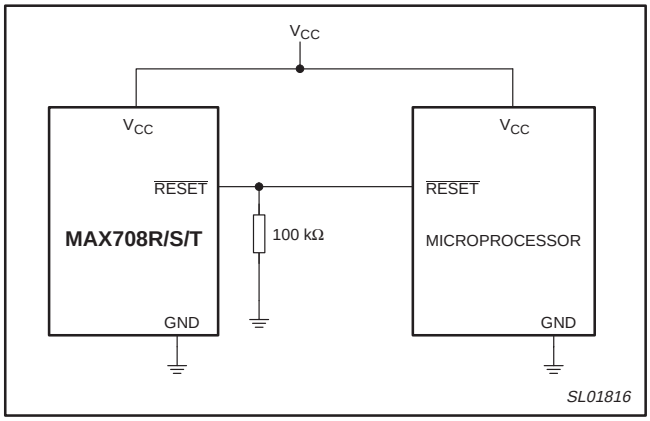


Figure 7. $\overline{RESET}$ valid to V_{CC} = Ground circuit.

Interfacing to a microprocessor with bi-directional reset pins

Microprocessors with bi-directional reset pins, such as the Motorola 68HC11 series, can be connected to the MAX708R/S/T $\overline{RESET}$ output. The bi-directional reset of the microprocessor functions both as a driven reset input and as an active reset driver.

To ensure a correct output on the MAX708R/S/T even when the microprocessor reset pin is in the opposite state, connect a 4.7 kΩ resistor between the reset pins as shown in Figure 8. This allows the microprocessor to issue commands to the system regardless of the state of the $\overline{RESET}$ pin.

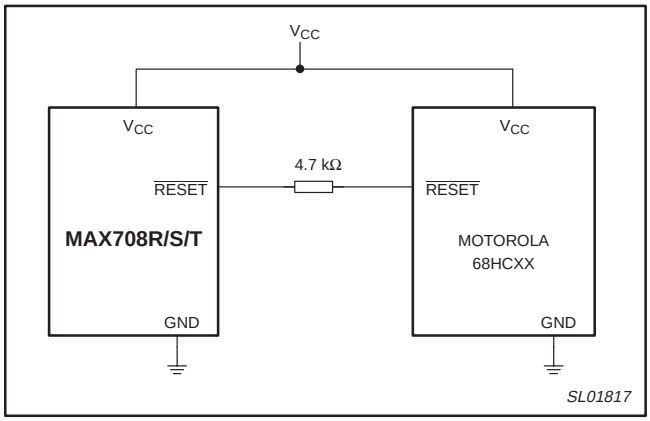


Figure 8. Interfacing to a microprocessor with bi-directional Reset I/O

PACKING METHOD

The MAX708R/S/T are packed in reels, as shown in Figure 9.

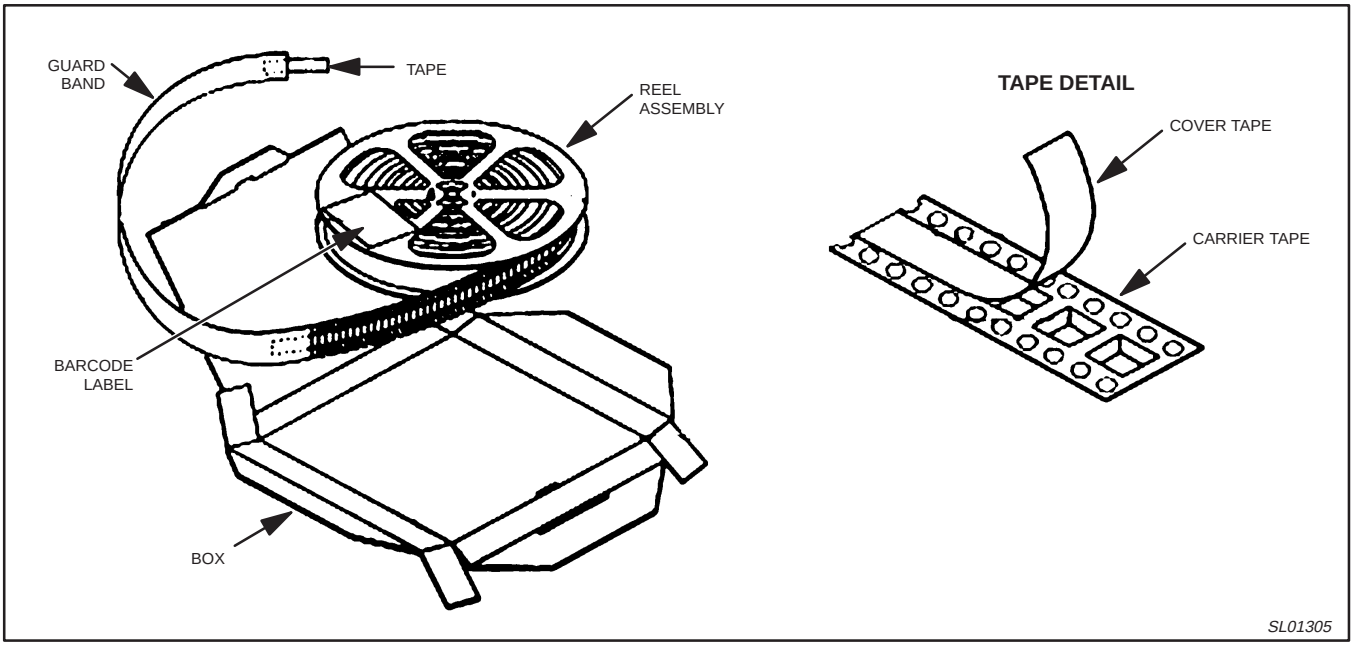
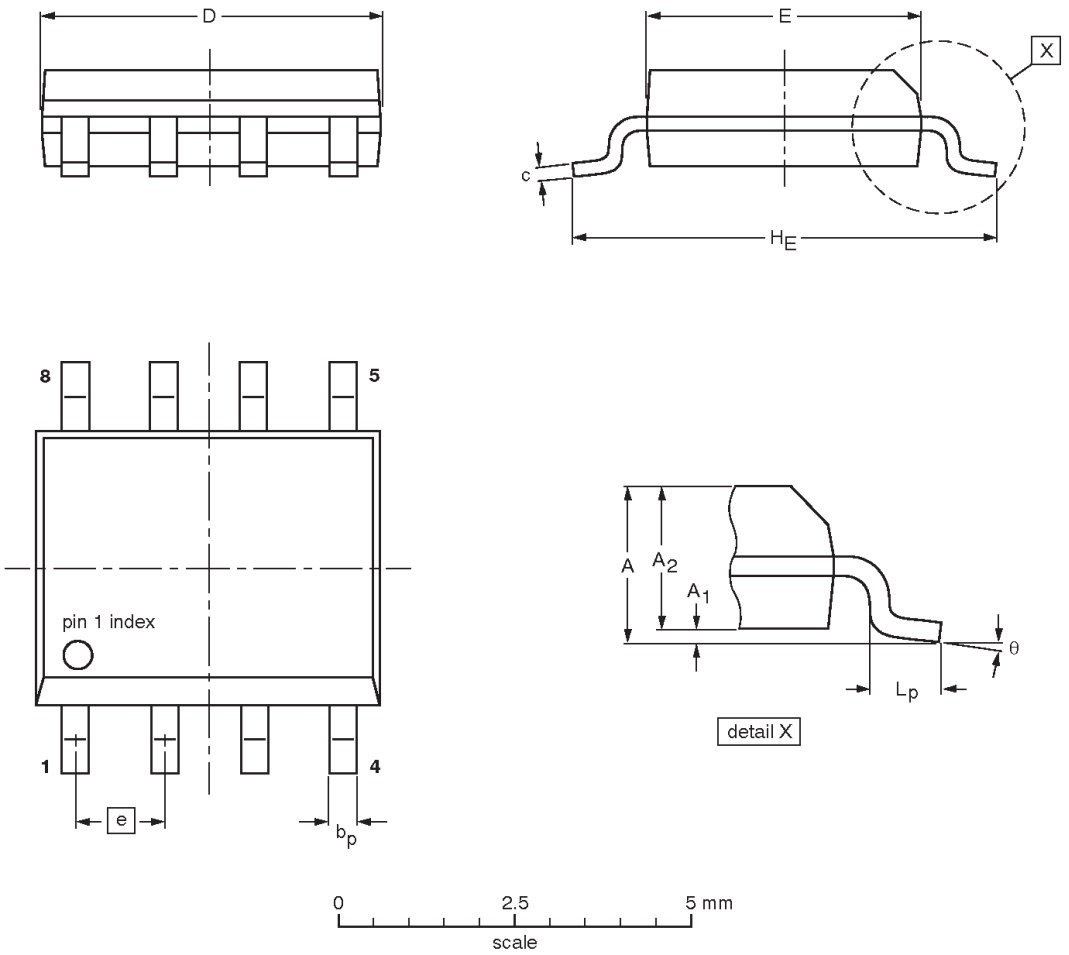


Figure 9. Tape and reel packing method.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOP005**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	b_p	c	D(1)	E(2)	e	H_E	L_p	θ
mm	1.73	0.25 0.10	1.45 1.25	0.51 0.33	0.25 0.19	4.95 4.80	4.0 3.8	1.27	6.2 5.8	1.27 0.38	8° 0°
inches	0.068	0.010 0.004	0.057 0.049	0.013 0.020	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.050 0.015	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOP005	076E03	MS-012				03-10-07

REVISION HISTORY

Rev	Date	Description
_4	20031015	**Product data (9397 750 12055); ECN 853–2354 30312 of 08 September 2003; supersedes data of 08 Aug 2003 (9397 750 11882).** Modifications: ● Change package outline drawing from SO8 (non-standard drawing) to SOP005 (offical drawing).
_3	20030808	**Product data (9397 750 11882); ECN 853–2354 30185 of 04 August 2003; supersedes data of 13 Feb 2003 (9397 750 10514).**
_2	20030213	**Product data (9397 750 10514); ECN 853–2354 29010 of 02 October 2002; supersedes data of 20 Jun 2002 (9397 750 10023).**
_1	20020620	**Product data (9397 750 10023); ECN 853–2354 28505 of 20 June 2002.**

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MAX708R/S/T

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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